POET TECHNOLOGIES INC.

Head Office:
Suite 501, 121 Richmond St. W
Toronto, ON, M5H 2K1
Phone: (416) 368-9411
Fax: (416) 861-0749

Operations Office:
P.O. Box 555
Storrs-Mansfield, CT 06268
Phone: (203) 612-2366

NEWS RELEASE

POET Technologies - Special Strategic Committee Update

Toronto, ON, and Storrs, CT, January 6, 2014 – POET Technologies Inc. (TSX-V: PTK, OTC: POETF) ("the Company") – developer of the proprietary planar-optoelectronic technology ("POET") platform for monolithic fabrication of integrated electronic and optical devices on a single semiconductor wafer – announced today the completion of the work of the Special Strategic Committee ("SSC") and the update of its published milestones. The Board of Directors has endorsed the Company's commercialization plan put forward by the SSC which is chaired by Executive Director Peter Copetti.

The SSC was established in June 2013 to investigate and initiate strategic alternatives for the commercialization of the POET technology platform using a multi-faceted approach based on discussions with potential industry partners. The following major recommendations of the SCC have been implemented:

- **A plan for establishing POET Development Alliances (PDA's)** – The Company is in discussion with several potential industry partners who have the necessary foundry infrastructure to take the POET technology to the manufacturing stage. The partnership roles encompass fab, tool and engineering resources as well as product and library development for future applications. Ideal partners will be producers of products which can incorporate the POET IP technology to provide the lowest power consumption and cost-effective industry disruptive system solutions.
- **Update to Milestone #5 and Milestone #7** – Both milestones are expected to be completed in the first 3 to 5 weeks of fiscal 2014. Significant progress has been made and both milestones are in the final phases of testing. Specific announcements will be made once the final testing is complete for both the Switching Laser Demonstration and the Optical Thyristor-based Infrared Detector and transistor combinations. Please see the new milestone schedule on our website.
- **Drive for Reduction of Feature Size to 100-nm Range (100nm), Milestone #8** – The Company has introduced new specific milestones associated with reducing feature size to the 100-nm range in scale. The POET team has realized submicron device operation down to 200-nm. The path to maintaining scaled operation down to 100nm has been identified. The Company has scheduled its Molecular Beam Epitaxy (MBE) to be shut down for cleaning and maintenance for a period of approximately 6 weeks after completing Milestones 5 and 7. After restarting the MBE, the Company expects to complete Milestone 8 and, accordingly, the timeline for the completion of this milestone has been moved to the first quarter of fiscal 2014. The 100-nm goal is matched to the state-of-the-art commercial III-V foundry capabilities and will demonstrate the greater than 50x speed improvement together with lower power consumption by a factor ranging from 4 to 10 depending on the application as compared to silicon at smaller nodes. Significant progress has been made on the completion of this milestone, although it has proven to be more difficult to achieve with the limited equipment available to POET. This highlights the importance of developing an alliance with a fab partner where repeating this milestone and improving it will be significantly easier with advanced lithography equipment standard for CMOS processing.

The revolutionary features of POET, monolithic integration of fully complementary transistors together with optical transmitters and transceivers are expected to disrupt current optical-electrical techniques with faster and less expensive monolithic IC solutions.

For the first time p-channel and n-channel devices can be integrated monolithically in a III/V semiconductor environment with the potential to fully replace all silicon based CMOS circuitry with higher speed and lower power. Fully integrated single device optical transceivers including the full range of digital data processing at speeds of 100Gbps and beyond will become a reality as they cannot be manufactured with current silicon technology for power, speed and cost reasons.

- **Design Kit Preparation**

  In addition to optimizing device parameters and yields, the next focus is to establish POET's technology design kits, a comprehensive design rules and device parameter library for POET, which will enable customers and partners to implement the POET process into their preferred foundries. It will also help licensed designs in a POET device ecosystem to proliferate and help existing silicon library functions to migrate to POET technology based circuitry in a minimum amount of time. In order for the POET team to focus on the preparation of technology design kits, the SCC has recommended that Milestone #9 and #10 be delayed and new completion dates for those milestones will be announced once a primary industry partner has been identified.

- **Operation Management and Program management**

  Besides the announced appointment of a Senior VP of Operations in November 2013, key management changes are underway at the research facility in Storrs, Connecticut. An efficient program management will be instituted and all documentation and design kit efforts will be handled on-site in a direct manner. This step underscores the current transition from research to development oriented activities within POET indicating the maturity of the technology at the present time. This management reporting structure will encourage the success of the finalization of the research stage of POET and provide for the long term substantiation and transfer of the involved IP. A new development team will be formed with partners to scale the POET Technology bringing it to a mature stage.

- **Globalization Plans**

  The Company is planning several initiatives to raise global awareness of POET and increase its global investor base. The Company intends to split monetization of the IP between multiple commercial markets and military applications and products to maximize returns of all the different aspects of the POET IP.

"The SSC's recommendations are the cornerstones of the Company's strategy for unlocking the value of POET's intellectual property," said Mr. Copetti. "Preparing for a development alliance with comprehensive documentation and full availability of a technology design kit will definitively enable industry partners to incorporate POET technology into their products, thereby shortening time-to-market for potential products, and helping to commercialize POET in the marketplace quickly. We are encouraged by our ongoing discussions to date with potential partners. As the general basic strategic goals recommended by the SSC have been adopted by the Board of Directors, the SSC will be dissolved and the Company will now change its focus from research to development, with a view to 2014 being the major recognition year for the POET technology."

The Company's proprietary POET platform has demonstrated planar monolithic standard CMOS fabrication of integrated circuit gallium arsenide (GaAs) based devices containing both electronic and optical elements on a single wafer.

By offering process IP with the potential for increased speed, density, reliability, lower power and costs, POET offers the semiconductor industry the ability to disrupt Moore's Law to the next cadence level, overcoming current silicon-based lithography and device bottlenecks in regards to speed and power. POET is a truly disruptive technology that is expected to change the roadmap capabilities for a broad range of applications and markets.

POET is offering a broad technology basis for several key markets. The development of technology design kits in fiscal 2014 will focus on a phased approach. Specific markets and partners will be targeted over time as technology design kits become available.

Refer to our website for the revised milestones schedule at www.poet-technologies.com or with the news release filed on SEDAR at www.sedar.com .

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About POET Technologies Inc.

POET Technologies is the developer of the POET platform for monolithic fabrication of integrated circuit devices containing both electronic and optical elements on a single semiconductor wafer. With head office in Toronto, Ontario, Canada, and operations in Storrs, CT, the Company, through ODIS Inc., a U.S. company, designs III-V semiconductor devices for military, industrial and commercial applications, including infrared sensor arrays and ultra-low-power random access memory. The Company has 30 patents issued and 9 patents pending for the POET process, with potential high speed and power-efficient applications in devices such as servers, tablet computers and smartphones. The Company's common shares trade on the TSX Venture Exchange under the symbol "PTK" and on

the OTCQX under the symbol "POETF". For more information please visit our websites at www.poet-technologies.com.

Dated: January 6, 2014

ON BEHALF OF THE BOARD OF DIRECTORS

Michel Lafrance, Secretary

For further information:
Christopher Chu, Grayling
Tel: (646) 284-9426
Email: poet@grayling.com

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This news release contains "forward-looking information" (within the meaning of applicable Canadian securities laws) and "forward -looking statements" (within the meaning of the U.S. Private Securities Litigation Reform Act of 1995). Such statements or information are identified with words such as "anticipate", "believe", "expect", "plan", "intend", "potential", "estimate", "propose", "project", "outlook", "foresee" or similar words suggesting future outcomes or statements regarding an outlook. Such statements include, among others, those concerning the Company's anticipated operational plans and activities including the following specific statements: (i) "Both milestones are expected to be completed in the first 3 to 5 weeks of fiscal 2014."; (ii) "The Company has scheduled its Molecular Beam Epitaxy (MBE) to be shut down for cleaning and maintenance for a period of approximately 10 weeks after completing Milestones 5 and 7. After restarting the MBE, the Company expects to complete Milestone 8 and, accordingly, the timeline for the completion of this milestone has been moved to the first quarter of fiscal 2014."; (iii) "The revolutionary features of POET, monolithic integration of fully complementary transistors together with optical transmitters and transceivers are expected to disrupt current optical-electrical techniques with faster and less expensive monolithical IC solutions." (iv) "For the first time p-channel and n-channel devices can be integrated monolithically in a III/V semiconductor environment with the potential to fully replace all silicon based CMOS circuitry with higher speed and lower power. Fully integrated single device optical transceivers including the full range of digital data processing at speeds of 100Gbps and beyond will become a reality as they cannot be manufactured with current silicon technology for power, speed and cost reasons." (iv) "This management reporting structure will encourage the success of the finalization of the research stage of POET and provide for the long term substantiation and transfer of the involved IP. A new development team will be formed with partners to scale the POET Technology to a mature stage." (v) "the Company will now change its focus from research to development, with a view to 2014 being the major recognition year for the POET technology." and (vi) "POET is a truly disruptive technology that is expected to change the roadmap capabilities for a broad range of applications and markets."

Such forward-looking information or statements are based on a number of risks, uncertainties and assumptions which may cause actual results or other expectations to differ materially from those anticipated and which may prove to be incorrect. Assumptions have been made regarding, among other things, management's expectations regarding future growth, plans for and completion of projects by the Company's third party relationships, availability of capital, and the necessity to incur capital and other expenditures. Actual results could differ materially due to a number of factors, including, without limitation, operational risks in the completion of the Company's anticipated projects, delays or changes in plans with respect to the development of the Company's anticipated projects by the Company's third party relationships, risks affecting the Company's ability to execute projects, risks inherent in operating in foreign jurisdictions, the ability to attract key personnel, and the inability to raise additional capital.

Although the Company believes that the expectations reflected in the forward-looking information or statements are reasonable, prospective investors in the Company's securities should not place undue reliance on forward-looking statements because the Company can provide no assurance that such expectations will prove to be correct. Forward- looking information and statements contained in this news release are as of the date of this news release and the Company assumes no obligation to update or revise this forward-looking information and statements except as required by law.