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NEWS RELEASE

POET Technologies Moves to Next Phase of Commercialization Plan, Endorses Recommendations of Special Strategic Committee

Toronto, ON, and Storrs, CT, August 16, 2013 – POET Technologies Inc. (TSX-V: PTK, OTC: POETF) (“the Company”) – developer of the proprietary planar-optoelectronic technology (“POET”) platform for monolithic fabrication of integrated electronic and optical devices on a single semiconductor wafer – announced today that its Board of Directors have endorsed the next phases of the Company’s commercialization plan put forward by the Special Strategic Committee (SSC) chaired by Executive Director Peter Copetti.

The multi-pronged approach is based on discussions with potential industry partners and advisers regarding the Company’s two key markets consisting of the military and commercial sector that have been identified as potential early adopters of the POET platform. Currently, while POET’s incorporation in military projects is proceeding well, and should provide value in several key verticals, significant value exists in adapting POET for mass production within a commercial semiconductor fab environment. The Company must rapidly move to the next phase of its commercialization plan, which includes addressing feature size and scalability requirements for commercial fabs.

The Board has therefore endorsed, and authorized the SSC to proceed on, these recommendations, including:

- **Establishing a POET Development Alliance (PDA)** – The Company will be establishing relationships with one or more industrial partners looking towards jointly adapting POET to commercial scale III-V implementation. Alliance partners will provide key input including intellectual assets, technical staff, manufacturing capability, and foundry resources. In addition to optimizing device parameters and yields, a near-term goal will be to establish comprehensive design rules and a device parameter library for POET, which will proliferate licensed designs in a POET device ecosystem.
- **Drive for Reduction of Feature Size to 100-nm Range (100NM)** – The Company will re-prioritize its technical roadmap by introducing specific milestones associated with reducing feature size from the sub-micron to the 100-nm range in scale, targeting 4Q2013 for that milestone. Consequently, the milestone for full optoelectronic integration on a single die will be re-scheduled to 2Q2014. Even without this full integration milestone, the 100-nm goal anticipates the cadence of commercial III-V foundry capabilities. This roadmap will focus the Company’s ODIS subsidiary on developmental work that will allow for scalable production within existing commercial fabs.
- **Adoption of a Shareholder Rights Plan (SRP)** – The Company will be structuring a special SRP to protect the potential value of the company, for all shareholders, during the period where discussions with potential partners may be taking place regarding PDA-related agreements, and as progress on the 100NM project continues.

“This move crystallizes the Company’s strategy for unlocking the value of our intellectual property,” said Mr. Copetti. “A development alliance with the right partners will definitely shorten time-to-market, and help evolve a design ecosystem for POET in the marketplace.”

Further SSC actions will be endorsed by the Board depending on the status of the above initiatives.

Mr. Copetti added, “While the new feature-size milestone is a challenge given our commitment to projects in our delivery pipeline, I believe the POET team is more than capable of achieving this goal. There is no doubt that POET can demonstrate its n- and p-channel capability to be a viable and scalable complement to silicon CMOS.”

The Company’s proprietary POET platform has demonstrated monolithic fabrication of integrated circuit gallium arsenide (GaAs) based devices containing both electronic and optical elements on a single wafer.

By offering components with the potential for increased speed, density, reliability, and lower costs, POET offers the semiconductor industry the ability to push Moore’s Law to the next cadence level, overcoming current silicon-based bottlenecks, and potentially changing the roadmap for a broad range of applications.

The POET platform is currently the basis for a number of key projects – including optical code division multiple access (OCDMA) devices for avionics systems, combined RF/optical phased arrays, optoelectronic directional couplers, and ultra-low-power random access memory (RAM).

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About POET Technologies Inc.

POET Technologies is the developer of the POET platform for monolithic fabrication of integrated circuit devices containing both electronic and optical elements on a single semiconductor wafer. With head office in Toronto, Ontario, Canada, and operations in Storrs, CT, the Company, through ODIS Inc., a U.S. company, designs III-V semiconductor devices for military, industrial and commercial applications, including infrared sensor arrays and ultra-low-power random access memory. The Company has 34 patents issued and 7 patents pending for the POET process, with potential high speed and power-efficient applications in devices such as servers, tablet computers and smartphones. The Company's common shares trade on the TSX Venture Exchange under the symbol "PTK" and on the OTCQX under the symbol "POETF". For more information please visit our websites at www.poet-technologies.com.

Dated: August 16, 2013

ON BEHALF OF THE BOARD OF DIRECTORS

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Such forward-looking information or statements are based on a number of risks, uncertainties and assumptions which may cause actual results or other expectations to differ materially from those anticipated and which may prove to be incorrect. Assumptions have been made regarding, among other things, management's expectations regarding future growth, plans for and completion of projects by the Company's third party relationships, availability of capital, and the necessity to incur capital and other expenditures. Actual results could differ materially due to a number of factors, including, without limitation, operational risks in the completion of the Company's anticipated projects, delays or changes in plans with respect to the development of the Company's anticipated projects by the Company's third party relationships, risks affecting the Company's ability to execute projects, risks inherent in operating in foreign jurisdictions, the ability to attract key personnel, and the inability to raise additional capital.

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